Specification (Replacement Paragraphs)

[0021] Bit line columns 110 are positioned alongside memory columns 104. Although FIGURE 1 illustrates a bit line column between each memory column, one skilled in the art will recognize that fewer bit line columns may be used in the invention. Bit line columns include bit lines 112. Bit lines 112 are conductors that carry electric current in order to generate a magnetic field that switches the polarity of the storage and readout layers in memory cells 106. Positioning bit lines 112 on the sides of memory cells ~~110~~ 106 reduces masking layers and process steps during memory fabrication. The invention is applicable to both 1T1MTJ and 1D1MTJ architecture to achieve 1TnMTJ and 1DnMTJ respectively.

[0022] In one embodiment, MRAM 100 is fabricated on a substrate which ~~conta [0023] ins~~ contains transistors 108 for addressing memory columns 104 and peripheral circuitry providing power, sensing, address registers, etc. (not shown). A silicon wafer may be used as a substrate, however, other materials with appropriate electrical and thermal properties may also be used as a substrate. The substrate must be such that the address transistor 108 and all the peripheral electronics can be built in it. It should have sufficient thermal conductivity to dissipate the heat produced by the MRAM cells. Other materials include SiO, SiC, polySi.

[0029] Layer 360 is a multilayer (2 repeats) of ~~(PtCo)~~ Co/Pt, which is the readout layer with lower coercivity (softer) than the storage layer. The Co may be approximately 0.5 nm thick and the Pt may be approximately 2 nm thick. In CoPt multilayers, the coercive field can be adjusted by varying the thickness of the layers and number of repeats. Generally, the coercive field increases with the number of repeats. One example of values of the coercive field for the readout and storage layers is 20 Oe for the readout layer and 60 Oe for the storage layer. The magnetic polarization of both the readout and storage layers are aligned during a memory write, while the magnetic polarization of only the readout layer is switched during a memory read.

[0033] FIGURE 4 is a diagram illustrating bit lines, magnetic fields and a memory cell. One method for performing a memory write, or storing data within MRAM 300 for out-of-plane magnetization, follows for memory cell 400. A memory write operation for in-plane magnetization differs and will be described below. Electric current flowing in opposite directions is feed to bit lines 410 and 420. Current in bit line 410 flows perpendicular and into the plane of FIGURE 4 while current in bit line 420 flows perpendicular and out of the plane of FIGURE ~~2~~ 4. Because the current is in opposite directions, the magnetic field around each of bit lines 410 and 420 are in opposite directions. The magnetic field around bit line 410 is clockwise while the magnetic field around bit line 420 is counter clockwise.

[0042] The resistance of memory column 104-1 is then determined by well know methods. Then, the direction of current through bit lines 112-1 and 112-2 is switched and the respective magnetic fields switch alignment of the magnetic polarization for readout layer 510, again without switching storage layer 520. Resistance of memory column 104-1 is again determined. Based on the difference in resistance between the first reading and the second, and the known magnetic polarization of readout layer 510 during the first and second reading, the magnetic polarization of storage layer ~~320~~ 520 becomes known. Resistance through a memory cell is lower when both the storage layer and readout layer are aligned in the same direction, higher when they are aligned in opposite directions.

[0051] Layer 670 is $Ni_{80}Fe_{20}$ that is approximately 25 nm thick. Layer 670 forms a free layer that is magnetostatically coupled parallel to the magnetization of the top NiFe layers of the adjacent bit lines. Layer 655' is an optional layer of $Co_{90}Fe_{10}$ if it is desired to have the free layer be a bilayer of $Co_{90}Fe_{10}/Ni_{80}Fe_{20}$ instead of a single layer 670 of just $Ni_{80}Fe_{20}$.

[0054] One method of performing a memory write, or storing data within MRAM 600 for ~~out-of-plane~~ in-plane magnetization, follows for memory cell 615. Electric current flowing (or pulsed) in the same direction is ~~feed~~ fed to bit lines 630-1 and 630-2. Current in bit lines 630-1 and 630-2 is shown flowing perpendicular and into the plane of FIGURE 6. Layer 670 on each of bit lines 630-1 and 630-2 act as cladding layers. Layers 670 are polarized in an Oersted magnetic field generated by the current through bit lines 630-1 and 630-2. Due to the parallel magnetostatic coupling between these layers 670 on bit lines 630-1 and 630-2, and layer 670 on memory cell 615, the magnetization of layer 670 in memory cell 615 aligns parallel to the magnetic field of bit lines 630-1 and 630-2.